## REMARKS

Claims 1-48 were pending. Claims 8-38, 40, and 41 have been withdrawn. Claims 49-52 were added to round out the scope of protection for the invention. No new matter has been added. Claims 1-7, 39, and 42-52 are currently pending.

At the outset, Applicant notes that the restriction/election requirement is being maintained. Applicant notes that claims 1 and 39 are generic to all embodiments of the invention, and if these claims are allowed then all claims should be examined and found allowable in this application.

Turning to the invention, defined by the elected claims, the present invention relates to a pixel cell having a strained silicon layer and the method of making and using the same. *See e.g.,* Abstract.

As such, independent claim 1 recites at least one pixel cell comprising, "a semiconductor substrate including a strained silicon layer at an upper portion thereof; and a photosensor for generating charge formed in an upper region of said semiconductor substrate."

Independent claim 39 recites, as amended, a method of forming a pixel cell comprising, "forming a semiconductor substrate; forming a strained silicon layer in association with an upper portion of said semiconductor substrate; and forming a photosensor for generating charge at said upper portion of said semiconductor substrate."

New independent claim 49 recites at least one pixel cell comprising, "a semiconductor substrate including a strained silicon layer at an upper portion thereof; a first charge collection region capable of collecting charge from impinging light formed below an upper surface of said strained silicon layer; [and] a second charge collection region for receiving charge from said first charge collection region, said second charge collection region formed below an upper surface of said strained silicon layer." Claim 49 further recites "a gate for electrically coupling said first and second charge collection regions, said gate being formed over said strained silicon layer."

New independent claim 51 recites, as amended, a method of forming a pixel cell comprising, "forming a semiconductor substrate; forming a strained silicon layer in association with an upper portion of said semiconductor substrate; forming a first charge collection region capable of collecting charge from impinging light below an upper surface of said strained silicon layer [and] forming a second charge collection region for receiving charge from said first charge collection region, said second charge collection region being formed below an upper surface of said strained silicon layer." Claim 51 further recites "forming a gate for electrically coupling said first and second charge collection regions over said strained silicon layer."

Claims 1-4, 7, 39, 42, 43, 43, and 48 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Freeman et al. The rejection is respectfully traversed.

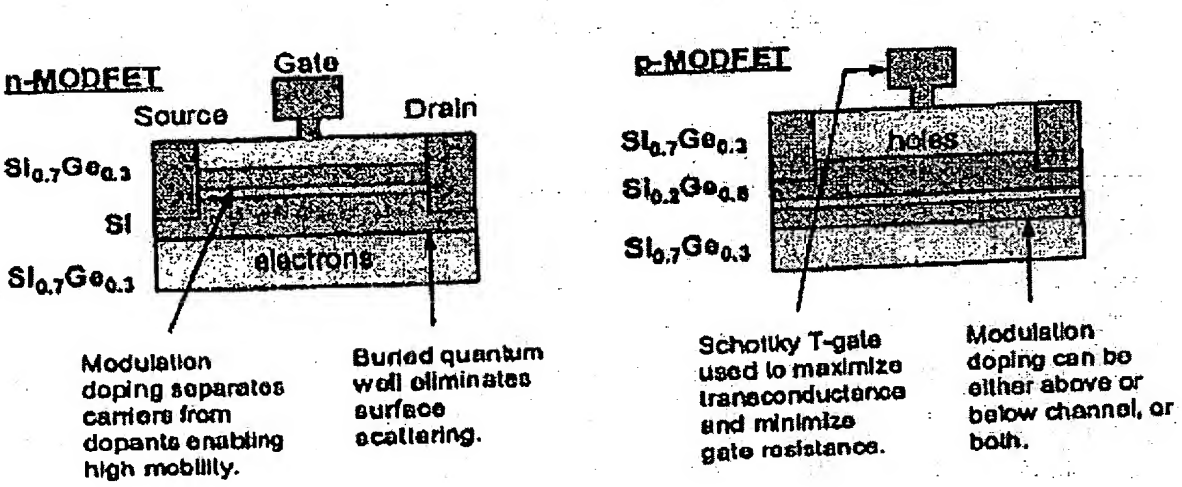
Freeman fails to disclose, teach, or suggest a pixel cell having "a semiconductor substrate including a strained silicon layer at an upper portion thereof; and a photosensor for generating charge formed in an *upper region* of said semiconductor substrate," as recited by claim 1.

Indeed, the Office Action admits that Freeman does not teach or disclose a strained silicon layer in use with a photosensor. Office Action at 3. Instead, the Office Action asserts that it would have been obvious for "one skilled in the art to safely relate the prior art with the claimed invention," and allegedly arrive at the claimed invention. The Office Action has not applied the proper test for obviousness; accordingly, the Office Action fails to make a *prima facie* case of obviousness.

Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. *See e.g.*, *In re Dembiczak*, 175 F.3d 994 (Fed. Cir. 1999); *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998); *Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc.*, 75 F.3d 1568, 1573 (Fed. Cir. 1996); and MPEP §§ 706.02(j) and 2143 *et seq.* Furthermore, the "[t]he teaching or suggestion to make the

claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." MPEP §706.02(j).

Applicant respectfully submits that there is no suggestion or motivation either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference. Indeed, Freeman's only depiction of a field effect transistor actually teaches away from "a semiconductor substrate including a strained silicon layer at an *upper portion* thereof"; Figure 17 of Freeman (reproduced below) shows the strained layer *between* a lower portion and an upper portion of a semiconductor substrate. Indeed, Freeman discloses that the "strained Si layer [is] sandwiched *between* relaxed $Si_{1-x}Ge_x$ layers." Freeman at 189 (emphasis added).




Freeman's use of strained silicon layers is limited to field effect transistors, and fails to disclose, teach, or suggest use of strained silicon layers in a pixel cell architecture, much less in association with a pixel cell photosensor. Accordingly, independent claim 1 and its dependent claims 2, 3, and 4, are allowable over Freeman.

Independent claim 39 is also not rendered obvious by Freeman. Freeman fails to disclose, teach, or suggest a method of forming a pixel cell comprising, *inter alia*, "forming a semiconductor substrate; [and] forming a strained silicon layer in association with an *upper portion* of said semiconductor substrate," as recited by claim 39.

As discussed above with respect to independent claim 1, there is no suggestion or motivation either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference to allegedly arrive at the claimed invention. Indeed, as discussed above, Freeman actually *teaches away* from forming "a strained silicon layer in association with an *upper portion* of said semiconductor substrate," as recited by claim 39.

For at least these reasons, independent claim 39, along with its dependent claims 42, 43, 44, and 48, is allowable over Freeman.

Claims 5 and 45 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Freeman et al. in view of Noguchi et al. The rejection is respectfully traversed.

As discussed above with respect to independent claims 1 and 39, Freeman does not disclose, teach, or suggest each and every limitation of claims 1 and 39. Noguchi does not cure the shortcomings of Freeman. Indeed, the Office Action cites Noguchi merely to "fill[] the gap" of the materials claimed in forming the silicon-germanium base layer. The Office Action once again fails to apply the proper test in combining references. As discussed above with respect to claim 1, it is improper to combine references based on applicant's disclosure, *see* MPEP §706.02(j); accordingly, the references cannot be combined without some motivation, which the Office Action has not provided.

Even if the references could be combined, which the Office Action has failed to show, the references, alone or in combination, fail to disclose, teach, or suggest each and every limitation of claims 1 and 39, from which claims 5 and 45 depend, respectively. Accordingly, Applicant respectfully submits that claims 5 and 45 are allowable over the references of record.

Claim 6 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Freeman et al. in view of Buchanan et al. The rejection is respectfully traversed.

As discussed above with respect to independent claim 1, Freeman does not disclose, teach, or suggest each and every limitation of claim 1. Buchanan does not cure the shortcomings of Freeman. Indeed, the Office Action cites Buchanan merely to "fill[] the gap" of "multilayered substrate[s]." Office Action at 6. The Office Action once again fails to apply the

proper test in combining references. As discussed above with respect to claim 1, it is improper to combine references based on applicant's disclosure, *see* MPEP §706.02(j); accordingly, the references cannot be combined without some motivation, which the Office Action has not provided.

Even if the references could be combined, which the Office Action has failed to show, the references, alone or in combination, fail to disclose, teach, or suggest each and every limitation of claim 1, from which claim 6 depends. Accordingly, Applicant respectfully submits that claim 6 is allowable over the references of record.

Claims 46 and 47 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Freeman et al. in view of Pomarade et al. The rejection is respectfully traversed.

As discussed above with respect to independent claim 39, Freeman does not disclose, teach, or suggest each and every limitation of claim 39. Pomarade does not cure the shortcomings of Freeman. Indeed, the Office Action relies on Pomarade for its alleged teaching of depositing silicon layers on the silicon-germanium base. Office Action at 7. The Office Action once again fails to apply the proper test in combining references. As discussed above with respect to claim 1, it is improper to combine references based on applicant's disclosure, *see* MPEP §706.02(j); accordingly, the references cannot be combined without some motivation, which the Office Action has failed to provide.

Even if the references could be combined, which the Office Action has failed to show, the references, alone or in combination, fail to disclose, teach, or suggest each and every limitation of claim 39, from which claims 46 and 47 depend. Accordingly, Applicant respectfully submits that claims 46 and 47 are allowable over the references of record.

New independent claim 49 is also not rendered obvious by the references of record, either alone or in combination. Specifically, none of the references of record disclose, teach, or suggest a pixel cell comprising, "a semiconductor substrate including a strained silicon layer at an upper portion thereof; a first charge collection region capable of collecting charge from impinging light formed below an upper surface of said strained silicon layer; [and] a second charge collection region for receiving charge from said first charge collection region, said

second charge collection region formed below an upper surface of said strained silicon layer," as recited by claim 49. Additionally, the references of record fail to disclose, teach, or suggest "a gate for electrically coupling said first and second charge collection regions, said gate being formed over said strained silicon layer," as recited by claim 49. Accordingly, Applicant respectfully submits that claim 49 and its dependent claim 50 are allowable over the references of record.

New independent claim 51 is also not rendered obvious by the references of record, either alone or in combination. Specifically, none of the references of record disclose, teach, or suggest a method of forming a pixel cell, comprising "forming a semiconductor substrate; forming a strained silicon layer in association with an upper portion of said semiconductor substrate; forming a first charge collection region capable of collecting charge from impinging light below an upper surface of said strained silicon layer [and] forming a second charge collection region for receiving charge from said first charge collection region, said second charge collection region being formed below an upper surface of said strained silicon layer," as recited by claim 51. Additionally, the references of record fail to disclose, teach, or suggest "forming a gate for electrically coupling said first and second charge collection regions over said strained silicon layer," as recited by claim 51. Accordingly, Applicant respectfully submits that claim 51 and its dependent claim 52 are allowable over the references of record.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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